OIPE JC49
APR 0 8 2004
PATENT & TRADEMARK OFFICE

FIG. 1

-- PRIOR ART --

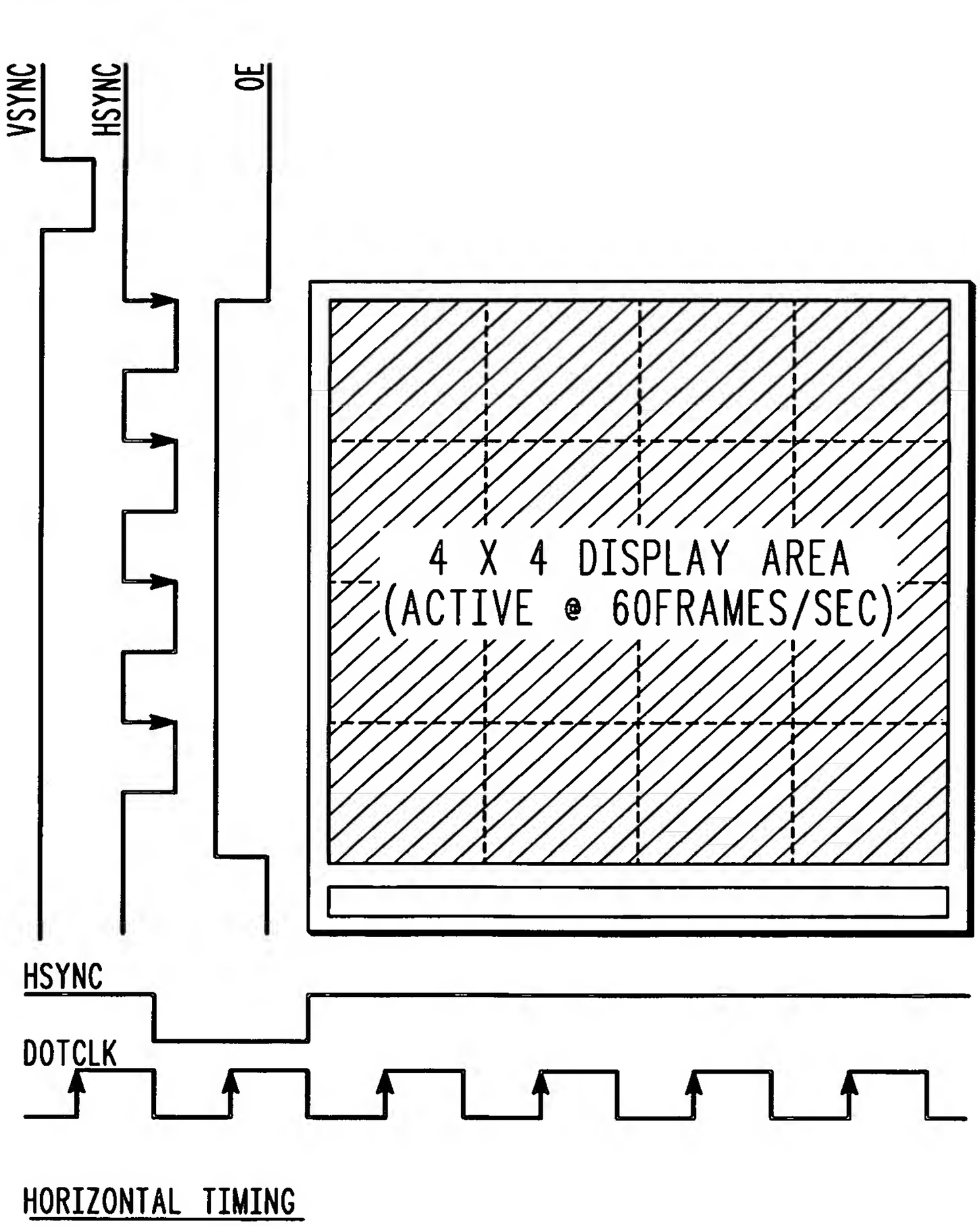


FIG. 2

-- PRIOR ART --

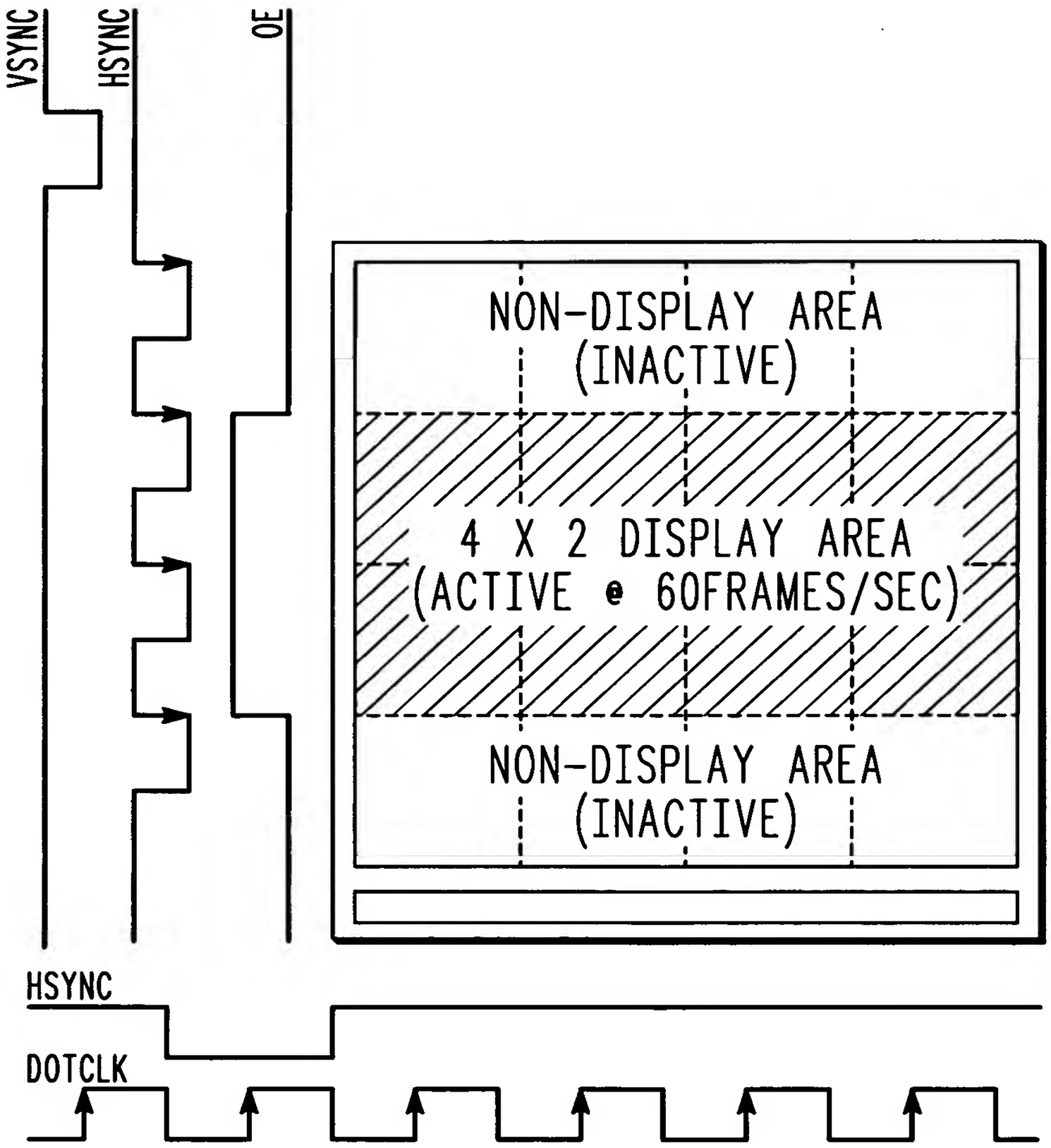
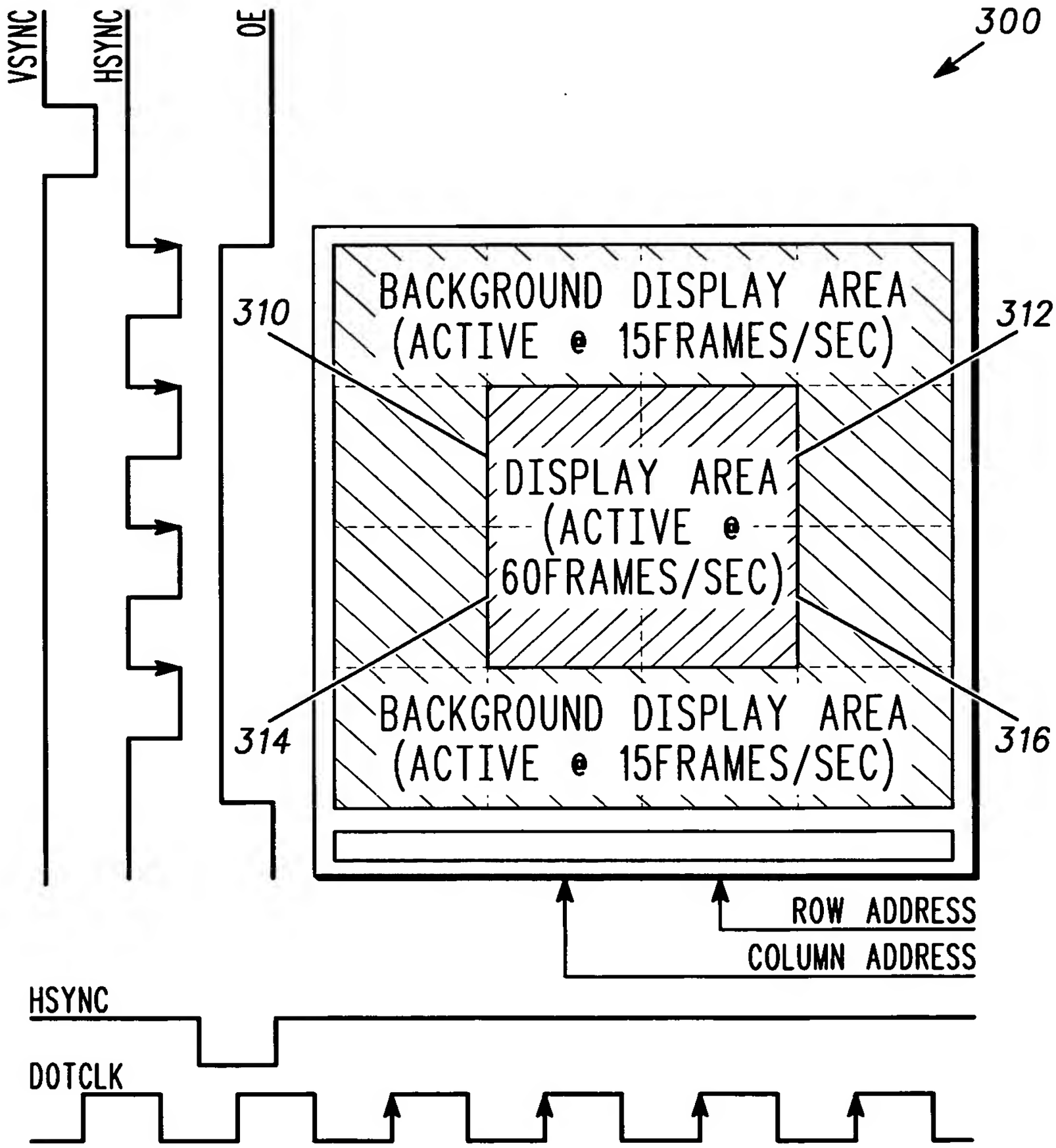


FIG. 3


300
VSYNC
HSYNC
OE
310
312
314
316
BACKGROUND DISPLAY AREA
(ACTIVE @ 15FRAMES/SEC)
DISPLAY AREA
(ACTIVE @
60FRAMES/SEC)
BACKGROUND DISPLAY AREA
(ACTIVE @ 15FRAMES/SEC)
ROW ADDRESS
COLUMN ADDRESS
HSYNC
DOTCLK

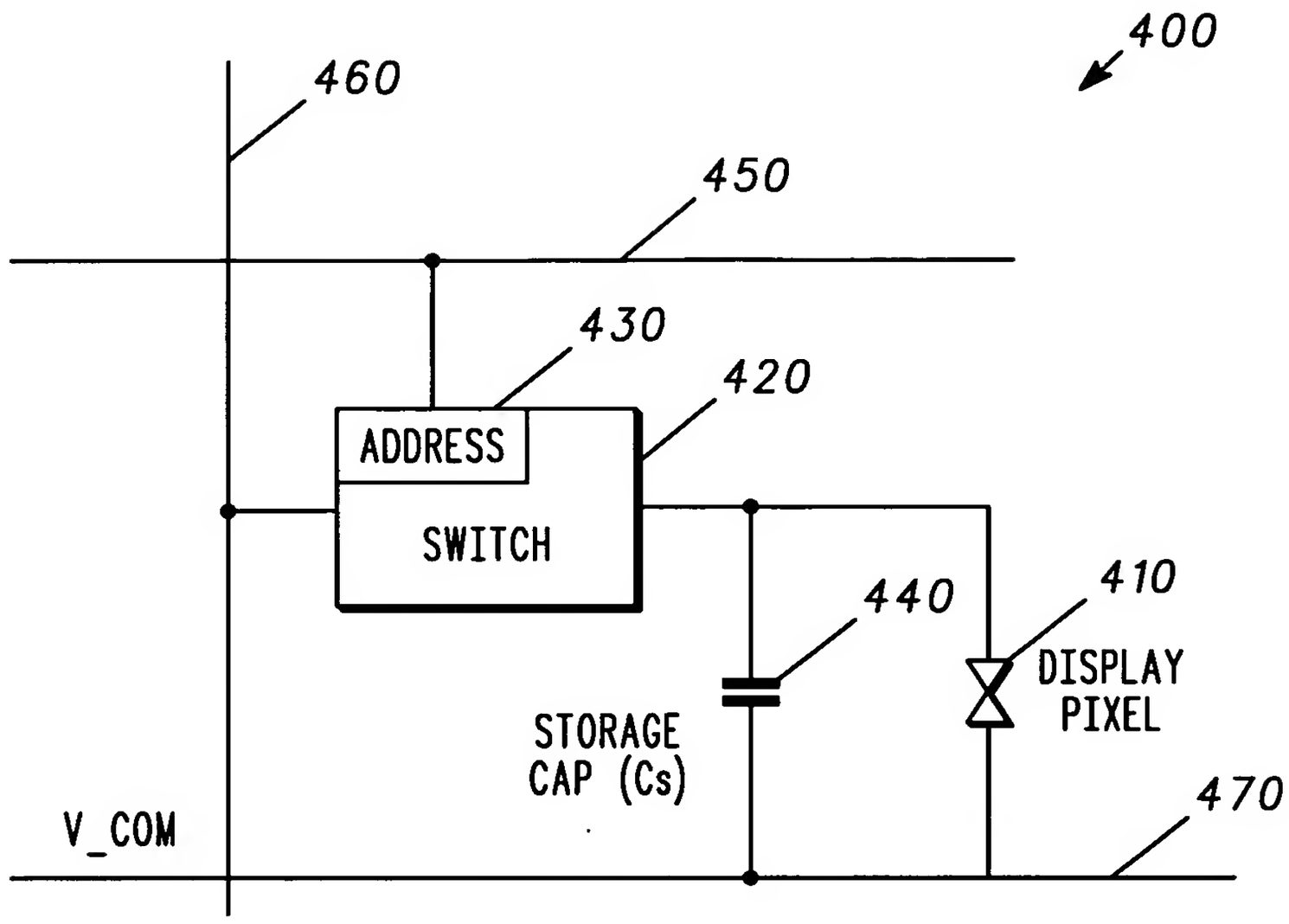

400
460
450
430
420
ADDRESS
SWITCH
440
410
DISPLAY
PIXEL
STORAGE
CAP (Cs)
470
V_COM

FIG. 4

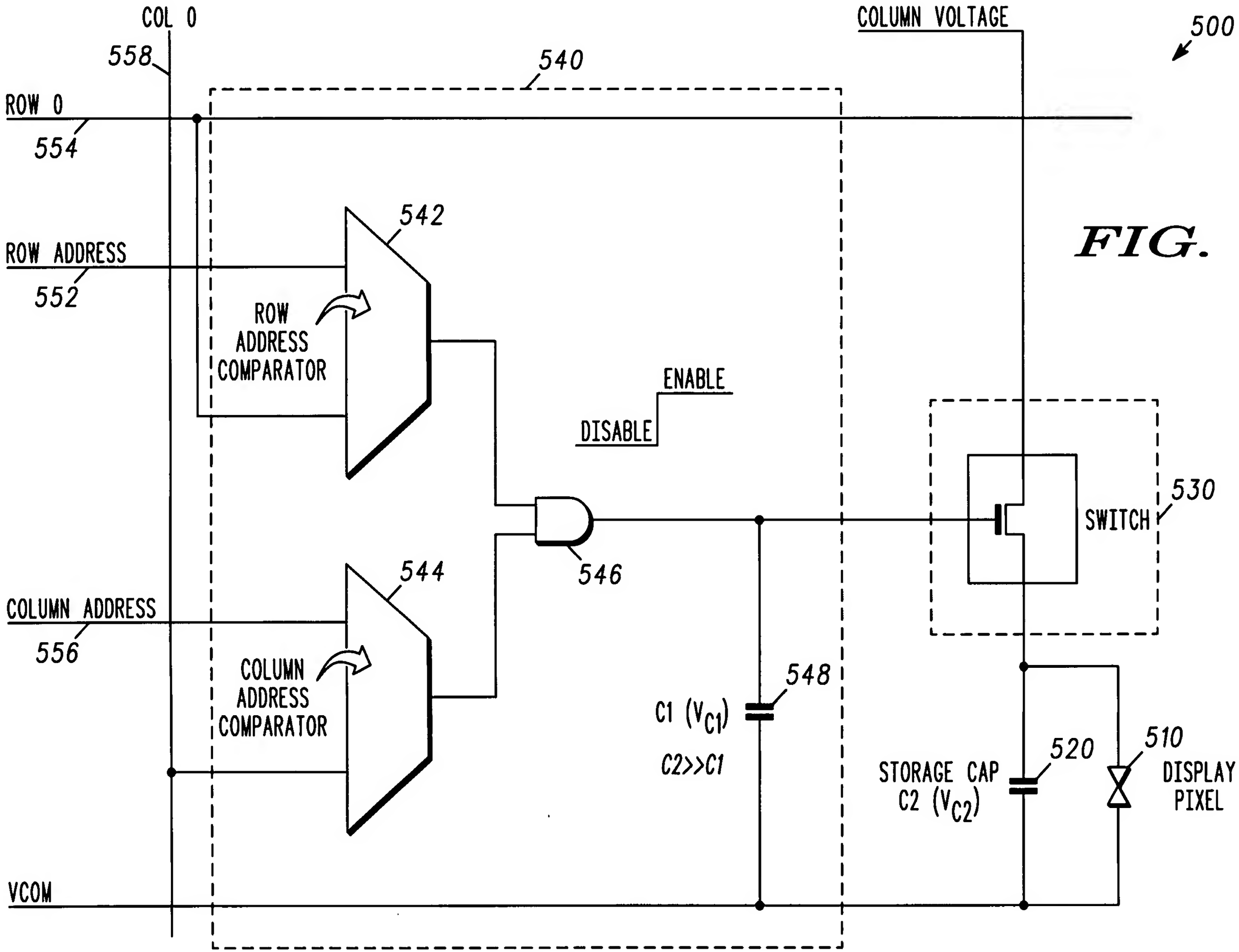

COL 0
558
540
COLUMN VOLTAGE
500
ROW 0
554
542
ROW ADDRESS
552
ROW ADDRESS COMPARATOR
ENABLE
DISABLE
530
SWITCH
546
544
COLUMN ADDRESS
556
COLUMN ADDRESS COMPARATOR
548
C1 (V_{C1})
C2>>C1
520
510
STORAGE CAP C2 (V_{C2})
DISPLAY PIXEL
VCOM

FIG. 5

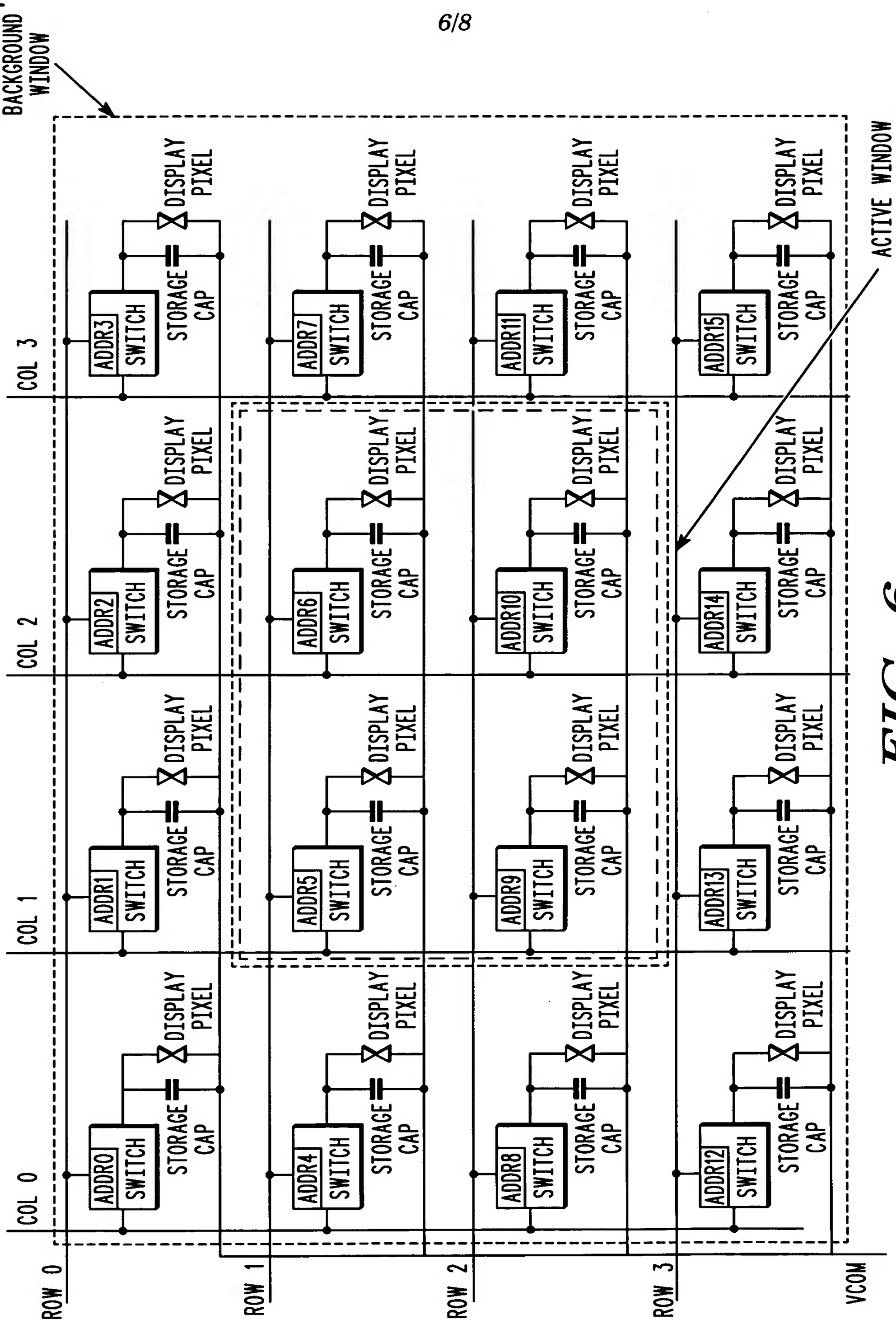
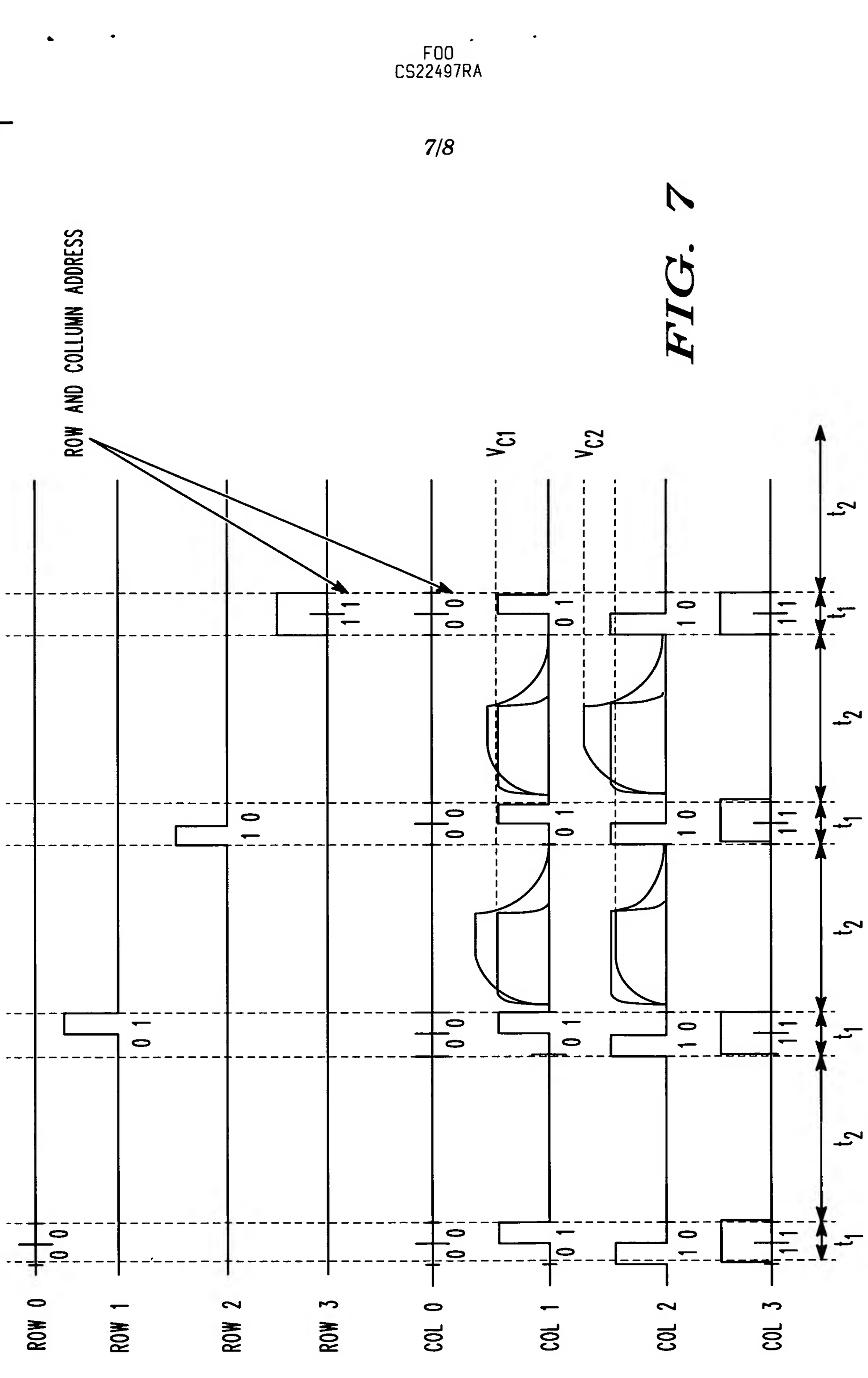

BACKGROUND WINDOW
ACTIVE WINDOW
COL 3
COL 2
COL 1
COL 0
ROW 0
ROW 1
ROW 2
ROW 3
VCOM
ADDR3
ADDR7
ADDR11
ADDR15
ADDR2
ADDR6
ADDR10
ADDR14
ADDR1
ADDR5
ADDR9
ADDR13
ADDR0
ADDR4
ADDR8
ADDR12
SWITCH
STORAGE CAP
DISPLAY PIXEL

FIG. 6

FIG. 7


ROW AND COLLUMN ADDRESS
V_{C1}
V_{C2}
t_1
t_2
ROW 0
ROW 1
ROW 2
ROW 3
COL 0
COL 1
COL 2
COL 3

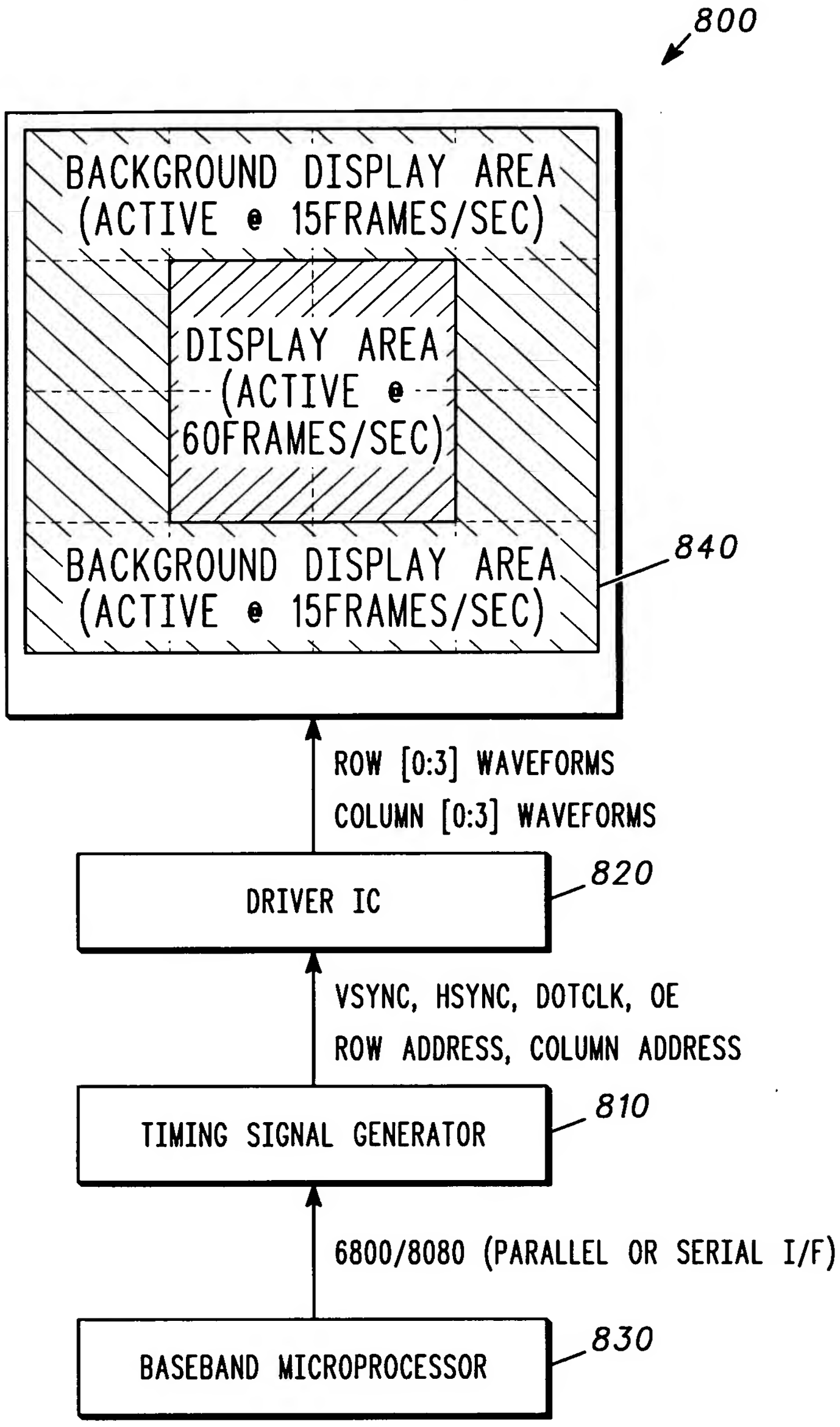

800
BACKGROUND DISPLAY AREA
(ACTIVE @ 15FRAMES/SEC)
DISPLAY AREA
(ACTIVE @
60FRAMES/SEC)
BACKGROUND DISPLAY AREA
(ACTIVE @ 15FRAMES/SEC)
840
ROW [0:3] WAVEFORMS
COLUMN [0:3] WAVEFORMS
DRIVER IC
820
VSYNC, HSYNC, DOTCLK, OE
ROW ADDRESS, COLUMN ADDRESS
TIMING SIGNAL GENERATOR
810
6800/8080 (PARALLEL OR SERIAL I/F)
BASEBAND MICROPROCESSOR
830

FIG. 8